IN THE CLAIMS

Please amend the claims as follows:

1.-26. (Canceled)

27. (New) A computerized method for generating a set of vectors for a logic design through computer-automated operations, the computerized method comprising:

identifying control logic for the logic design and excluding the control logic from the set of vectors, the control logic generating control input for the logic design, the control input including at least one control signal;

grouping at least one instance of a first template in the logic design based on the control input and a databus input for the logic design to generate a first vector of the set of vectors, the databus input including at least one databus identifier; and

grouping at least one instance of a second template based on circuit connectivity of the logic design to generate a second vector of the set of vectors.

28. (New) The computerized method of claim 27, wherein grouping at least one instance of the second template is performed after grouping at least one instance of the first template is performed.

29. (New) The computerized method of claim 27 further comprising:

grouping at least one instance of the second template to generate a third vector of set of vectors based on the circuit connectivity, wherein the second vector and the third vector include different instances of the second template.

30. (New) The computerized method of claim 27 further comprising:

grouping at least one instance of a third template in the logic design based on at least one of the control input, the databus, and the circuit connectivity to generate a third vector of the set of vectors, wherein grouping at least one instance of the second template is performed

after grouping at least one instance of the first template is performed and after grouping at least one instance of the third template is performed.

31. (New) The computerized method of claim 27, wherein at least one of the first template and the second template is a multi-output template.

32. (New) The computerized method of claim 27, wherein the logic design is for a datapath circuit.

33. (New) A machine-readable medium comprising instructions, which when implemented by one or more processors perform the following operations:

identifying control logic for the logic design and excluding the control logic from the set of vectors, the control logic generating control input for the logic design, the control input including at least one control signal;

grouping at least one instance of a first template in the logic design based on the control input and a databus input for the logic design to generate a first vector of the set of vectors, the databus input including at least one databus identifier; and

grouping at least one instance of a second template based on circuit connectivity of the logic design to generate a second vector of the set of vectors.

34. (New) The machine-readable medium of claim 33, wherein grouping at least one instance of the second template is performed after grouping at least one instance of the first template is performed.

35. (New) The machine-readable medium of claim 33, wherein the instructions when implemented further perform the following operation:

grouping at least one instance of the second template to generate a third vector of set of vectors based on the circuit connectivity, wherein the second vector and the third vector include different instances of the second template.

36. (New) The machine-readable medium of claim 33, wherein the instructions when implemented further perform the following operation:

grouping at least one instance of a third template in the logic design based on at least one of the control input, the databus, and the circuit connectivity to generate a third vector of the set of vectors, wherein grouping at least one instance of the second template is performed after grouping at least one instance of the first template is performed and after grouping at least one instance of the third template is performed.